

CLAIMS

What is claimed is:

1. An embedded semiconductor product comprising:

a semiconductor substrate;

a first isolation trench adjoining a logic cell active region of the semiconductor substrate;

and

a second isolation trench adjoining a memory cell active region of the semiconductor substrate, wherein the second isolation trench is deeper than the first isolation trench.

2. The product of claim 1 wherein the first isolation trench is formed to a depth of from about 2500 to about 5000 angstroms.

3. The product of claim 1 wherein the second isolation trench is formed to a depth of from about 4000 to about 9000 angstroms.

4. The product of claim 1 further comprising a first isolation region formed within the first isolation trench and a second isolation region formed within the second isolation trench.

5. The product of claim 4 further comprising a storage capacitor comprising a storage capacitor plate layer formed at least in part penetrating into the second isolation region.

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6. The product of claim 5 wherein the storage capacitor comprises a sidewall of the second trench, a capacitor dielectric layer formed thereupon and the capacitor plate layer formed thereupon.

7. A method for fabricating an embedded semiconductor product comprising:

providing a semiconductor substrate;

forming a first isolation trench adjoining a logic cell active region of the semiconductor substrate; and

forming a second isolation trench adjoining a memory cell active region of the semiconductor substrate, wherein the second isolation trench is deeper than the first isolation trench.

8. The method of claim 1 wherein the semiconductor substrate is a silicon semiconductor substrate.

9. The method of claim 1 wherein the first isolation trench is formed to a depth of from about 2500 to about 5000 angstroms.

10. The method of claim 1 wherein the second isolation trench is formed to a depth of from about 5000 to about 6000 angstroms.

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11. The method of claim 1 further comprising forming a first isolation region formed within the first isolation trench and forming a second isolation region formed within the second isolation trench.

12. The method of claim 4 further comprising forming a storage capacitor comprising a storage capacitor plate layer formed at least in part penetrating into the second isolation region.

13. The method of claim 5 wherein the storage capacitor comprises a sidewall of the second trench, a capacitor dielectric layer formed thereupon and the capacitor plate layer formed thereupon.

14. A method for fabricating an embedded semiconductor product comprising:

providing a semiconductor substrate;

forming simultaneously a first isolation trench adjoining a logic cell active region of the semiconductor substrate and a second isolation trench adjoining a memory cell active region of the semiconductor substrate; and

further etching the second isolation trench but not the first isolation trench such that the second isolation trench is deeper than the first isolation trench.

15. The method of claim 1 wherein the semiconductor substrate is a silicon semiconductor substrate.

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16. The method of claim 1 wherein the first isolation trench is formed to a depth of from about 2500 to about 5000 angstroms.

17. The method of claim 1 wherein the second isolation trench is formed to a depth of from about 4000 to about 9000 angstroms.

18. The method of claim 1 further comprising forming a first isolation region formed within the first isolation trench and forming a second isolation region formed within the second isolation trench.

19. The method of claim 4 further comprising forming a storage capacitor comprising a storage capacitor plate layer formed at least in part penetrating into the second isolation region.

20. The method of claim 5 wherein the storage capacitor comprises a sidewall of the second trench, a capacitor dielectric layer formed thereupon and the capacitor plate layer formed thereupon.